REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claims 8-10 stand rejected under 35 U.S.C. 103(e) as allegedly being anticipated by U.S. Patent No. 5,821,137 to Wakai. Claim 11 stands rejected based on Wakai in view of U.S. Patent No. 4,613,382 issued to Katayama.

In response to this rejection, all of the independent claims have been amended to add the recitation that a pair of portions have the same conductivity type as the second source and drain regions. This is shown by all of the thin film transistors in the specification.

Wakai shows that a region which is adjacent to the source and drain region has a different conductivity type than the source and drain regions in the active layer. For example, see Fig. 4E of Wakai, et al. Because of this, the current characteristics of the thin film transistor are relatively low. For these reasons, the structure which is suggested by Wakai would be effective to reduce the off current, but would not be especially suitable for a thin film transistor that requires high on-current characteristics. For example, a thin film transistor in a driver circuit in an active matrix display would not operate well with the Wakai system, since these systems

often require high on-current characteristics. Therefore, Wakai's system would not work well for a thin film transistor in a driver circuit in an active matrix display.

The thin film transistor of the present invention has a different structure with a high on-current. This is very different than Wakai, and produces advantages thereover as described above. Hence, it is respectfully suggested that this amendment obviates the rejection under §102.

Claim 11 stands rejected under 35 U.S.C. 103(a) as allegedly being obvious over Wakai in view of Katayama. The amendment made above obviates this rejection.

Claims 1-11 stand rejected under judicially created obviousness-type double patenting based on U.S. Patent No. 6,194,762. However, it is respectfully suggested that '762 does not refer to the feature of the conductivity types of the pair of portions. This amendment which is now made to the claims therefore obviates the rejection under obviousness-type double patenting.

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

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Respectfully submitted,

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VERSION TO SHOW CHANGES MADE

In the Claims:

The claims have been amended as follows.

1. (Amended) An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least a first thin film transistor and a second thin film transistor;

said first thin film transistor comprising:

a first semiconductor layer having first source and drain regions, a pair of lightly-doped regions and a first channel forming region therebetween; and

a first gate electrode adjacent to said first channel forming region with a first gate insulating layer interposed therebetween, and

said second thin film transistor comprising:

a second semiconductor layer having second source and drain regions and a second channel forming region therebetween; and

a second gate electrode adjacent to said second channel forming region with a second gate insulating layer interposed therebetween,

wherein said second channel forming region directly contacts with said second source and drain regions,

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said second source [region] and [said second] drain [region] regions respectively, [and]

wherein said pair of portions have the same conductivity type as said second source and drain regions, and

wherein an electrode is connected to at least one of said pair of portions.

2. (Amended) An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least a first thin film transistor and a second thin film transistor;

said first thin film transistor comprising:

a first semiconductor layer having first source and drain regions, a pair of lightly-doped regions and a first channel forming region therebetween; and

a first gate electrode adjacent to said first channel forming region with a first gate insulating layer interposed therebetween, and

said second thin film transistor comprising:

a second semiconductor layer having second source and drain regions and a second channel forming region therebetween; and

a second gate electrode adjacent to said second channel forming region with a second gate insulating layer interposed therebetween,

wherein said second channel forming region directly contacts with said second source and drain regions [contain] containing a p-type impurity [and directly connect with said second channel forming region],

wherein a pair of portions containing n-type and p-type impurities and having a p-type conductivity are formed adjacent to said second source [region] and [said second] drain [region] regions respectively, and

wherein an electrode is connected to at least one of said pair of portions.

3. (Amended) An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least one thin film transistor, said thin film transistor comprising:

a semiconductor layer having [a] source and drain regions and a channel forming region therebetween; and

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said channel forming region directly contacts with said [second] source and drain regions,

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said source and drain [region] regions respectively, [and]

wherein said pair of portions have the same conductivity type as said source and drain regions, and

wherein an electrode is connected to at least one of said pair of portions.

4. (Amended) An active matrix display device comprising:

an active matrix circuit and a driver circuit formed over a substrate;

said driver circuit including at least one thin film transistor, said thin film transistor comprising:

a semiconductor layer having [a] source and drain regions and a channel forming region therebetween; and

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said channel forming region directly contacts with said source and drain regions [contain] containing a p-type impurity [and directly connect with said channel forming region],

wherein a pair of portions containing n-type and p-type impurities and having a p-type conductivity are formed adjacent to said source and drain [region] regions respectively, and

wherein an electrode is connected to at least one of said pair of portions.

5. (Amended) An active matrix display device according to any one of claims 1 to [4] 2, wherein said first source and drain regions contain an n-type impurity.

6. (Amended) An active matrix display device according to any one of claims 1 to [4] 2, wherein said first channel forming region and said second channel forming [regions] region contain an impurity imparting one conductivity.

7. (Amended) An active matrix display device according to any one of claims 1 to [4] 2, wherein said first semiconductor layer and said second semiconductor [layers] layer contain hydrogen and halogen.

8. (Amended) A semiconductor device having at least one thin film transistor formed over a substrate, said thin film transistor comprising:

a semiconductor layer having [a] source and drain regions and a channel forming region therebetween; and

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said channel forming region directly contacts with said [second] source and drain regions,

wherein a pair of portions containing n-type and p-type impurities are formed adjacent to said source and drain [region] regions respectively, [and]

wherein said pair of portions have the same conductivity type as said source and drain regions, and

wherein an electrode is connected to at least one of said pair of portions.

9. (Amended) A semiconductor device having at least one thin film transistor formed over a substrate, said thin film transistor comprising:

a semiconductor layer having [a] source and drain regions and a channel forming region therebetween; and

a gate electrode adjacent to said channel forming region with a gate insulating layer interposed therebetween,

wherein said channel forming region directly contacts with said source and drain regions [contain] containing a p-type

impurity [and directly contact with said channel forming region],

wherein a pair of portions containing n-type and p-type impurities and having a p-type conductivity are formed adjacent to said source and drain [region] regions respectively,

wherein an electrode is connected to at least one of said pair of portions.

10. (Amended) A semiconductor device according to [either] any one of [claim 8 or 9] claims 3, 4, 8 and 9, wherein said channel forming region contains an impurity imparting one conductivity.

11. (Amended) A semiconductor device according to [either] any one of [claim 8 or 9] claims 3, 4, 8 and 9, wherein said semiconductor layer contains hydrogen and halogen.